3D characterization of advanced nanoelectronic devices

Narciso Gambacorti
CEA Leti

In modern nanoelectronic devices, to increase their performance, decrease the power consumption and decrease their dimension (increase density), one of the main trend is to use more and more three dimensional architectural geometry.This approach can be used both at the device scale (the so-called More-Moore roadmap) with the development of novel geometries for the device ranging from finFET to stacked nanowires or at chip level where three dimensional integration of heterogeneous systems (the so-called More-then-Moore roadmap) is the driving force to increase the functionality of the chips. It is evident that in this contest is of paramount importance the “three dimensional” characterization of these devices/structures. However, we need to be able to perform these characterizations at different lengthscale: from the atomic-scale (for the characterization of the more advanced devices) up to the micron-scale (for the characterization of the more complex integrated systems-onchip).