

Tommaso Vali is the Senior Director at Micron Semiconductor Italy and has the responsibility of the Avezzano, Padova and Catania Design centers for the design on NVM memories in Europe. He received a degree in electronic engineering at the University of Rome "La Sapienza" in 1987, since then he worked at Texas Instruments and moved to TI Avezzano R&D department as a designer Engineer of MOS circuits in 1994.

He became Senior designer and Distinguished Member of Technical Staff at TI in 1996. In 1998, following Micron Technology Inc. acquisition of all TI memory business, he had increasing responsibilities in the design center as team leader and design Manager for Wireless NOR. Since 2004, he is the Director of the Avezzano design center for NAND design. In 2008, he set up the Padua design center that joined the Avezzano team in NVM design activities. In 2010, the two teams worked to the the first 32Gb 3bpc NAND memory at 32nm in the industry (presented in 2010 at ISSCC, S.Francisco). Since 2015, the Catania design team joined the organization and worked together within the NVM DE teams to the release of a 256Gb 2b/cell 3D NAND and of a 768Gb 3b/cell 3D Floating Gate NAND Flash memory (presented in 2016 at the ISSCC, S.Francisco)