Transistors and memories based on 2D materials for integrated circuits dedicated to machine learning

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Transistors and non-volatile memories based on lateral and vertical heterostructures of two-dimensional materials have the potential to outperform CMOS in terms of energy per computing operation and energy per memory access., as indicated by multi-scale devise simulations. They also are particularly well suited for logic-in-memory architectures, that are particularly relevant for machine learning applications on devices as the edge of the internet of things.

In this talk we will discuss the options for transistor structures and non-volatile memory concepts, and their corresponding expected performance using as a benchmark the foreseeable evolution of CMOS technology for emerging applications.

Lateral heterostructure FETs emerge as the most promising candidates for logic, whereas floating-gate non-volatile memories based on vertical heterostructures for the gate stack and lateral heterostructures for the channel appear as the most promising candidates for the storage of frequently used variables, such as neural network weights.